high speed DRAM to the write register.

5. The high speed DRAM of claim 4, wherein an eighth data bus (8) couples the write register to outside data buses.

6. The high speed DRAM of claim 5, wherein a multiplexer (700) switches between inputs received from the sixth data bus from the read register and the eight data bus from the write register, and outputs data onto a ninth data bus (9) coupled to the outside data buses.

7. The high speed DRAM of claim 6, wherein a read buffer (800) couples the read register to the DRAM memory through a tenth data bus.

8. The high speed DRAM of claim 7, wherein an eleventh data bus couples the DRAM memory to a write buffer which is coupled through the third data bus to the write register.

9. The high speed DRAM of claim 7, wherein the first, second, third, fourth, fifth, tenth, and eleventh data buses all have the same first wide data bandwidth.

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10. The high speed DRAM of claim 6, wherein the sixth, seventh, eight, and ninth data buses all have the same second narrow data bandwidth.